APPENDIX

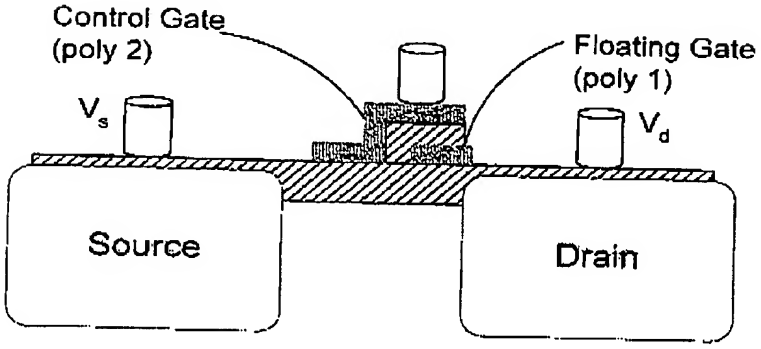

Figure 1

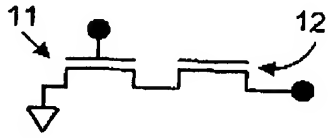

Figure 1A

Figure 1B

SG EE	Erase	Program	Read
SG Wordline (WL)	-17 V (-12 V)	Vt	Vref
Bitline (BL)	Vss (5V)	12 V	Vdd
Source Line (SR)	Vss	Vss	Vss

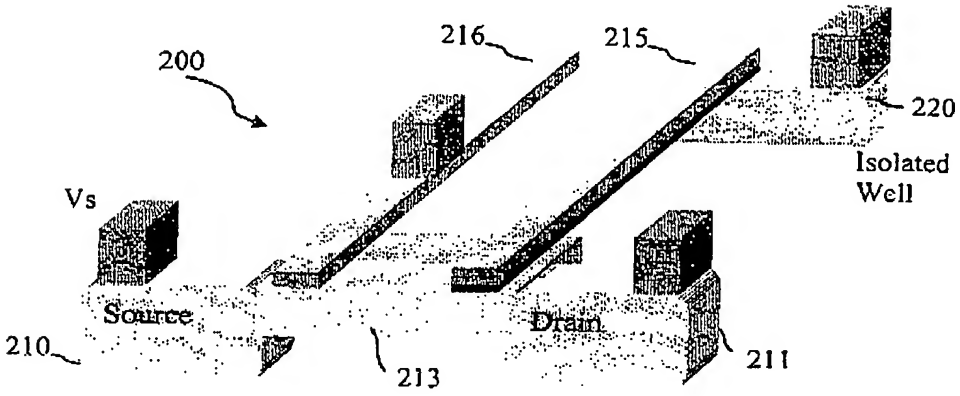

Figure 2A

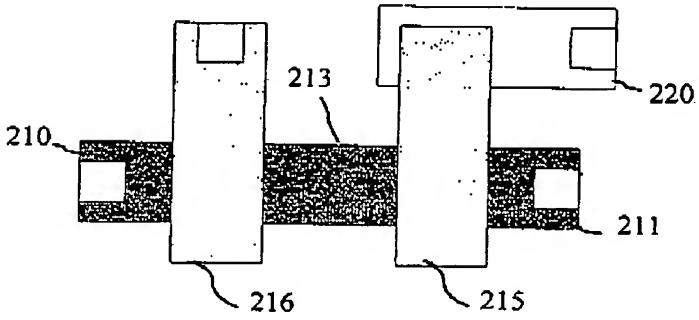

Figure 2B

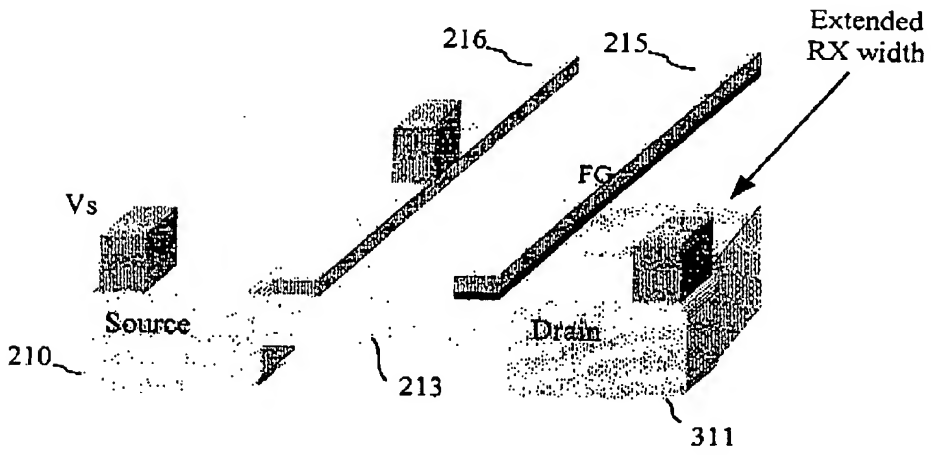

Figure 3A

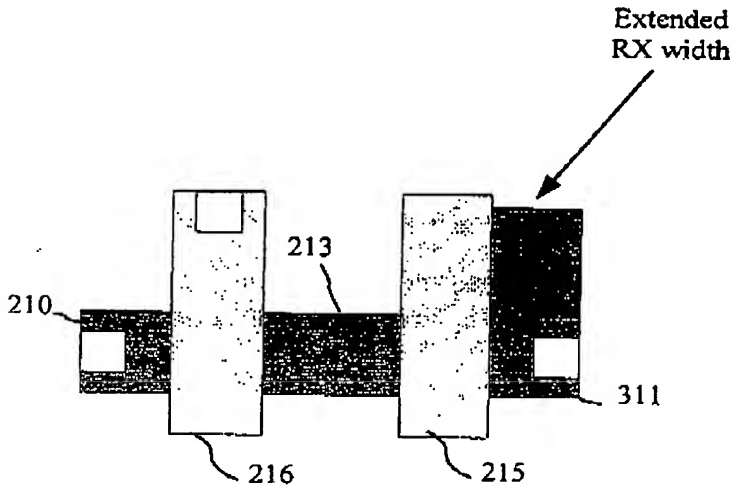

Figure 3B

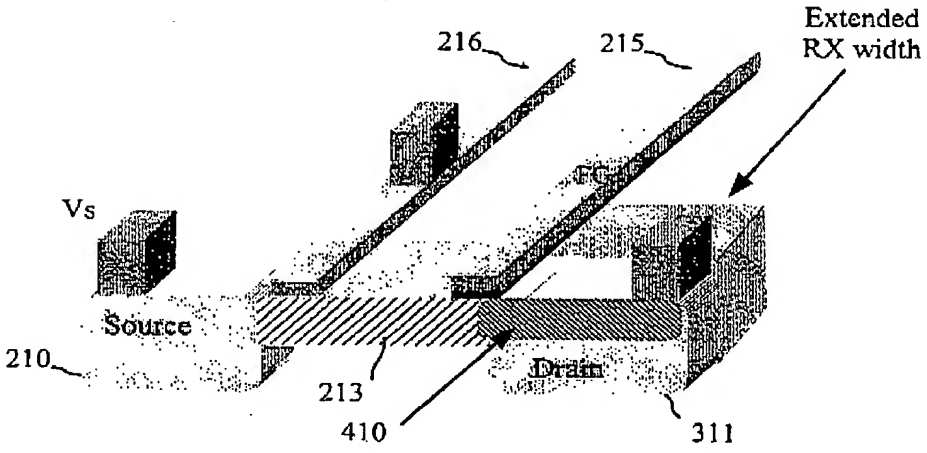

Figure 4A

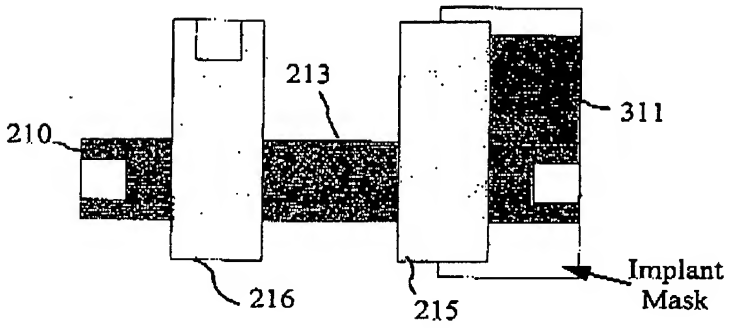

Figure 4B

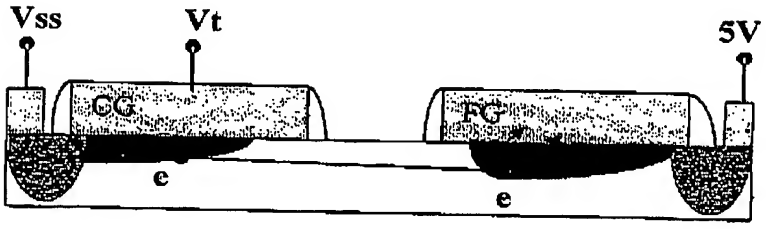

Figure 5A

NVM Fuse	Erase	Program	Read
Selected Wordline	-5 V	Vt	Vref
(BL) (+ iso-well	5 V	5 V	Vdd
Source	Vss	Vss	Vss

Figure 5B

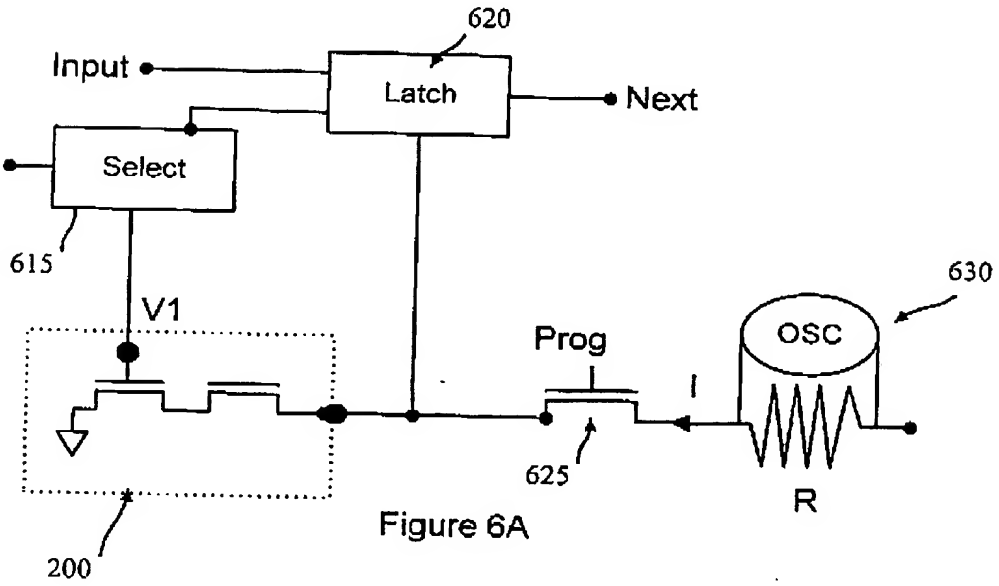

Figure 6A

NVM fuse	Erase	Program	Read
Select (WL)	-5 V	Vt	Vref
Latch BL (Prog FET)	5V	5 V (on)	Vdd (off)
Source	Vss	Vss	Vss

Figure 6B